CLAIMS

What is claimed is:

1. A method of forming an ILD dielectric layer stack to allow improved local interconnect formation comprising the steps of:

providing a semiconductor substrate comprising CMOS transistors comprising gate electrode portions;

depositing a first layer comprising phosphorous doped SiO_2 over the semiconductor substrate to a thickness sufficient to fully cover the gate electrode portions including intervening gaps;

depositing a second layer of undoped SiO_2 over and contacting the first layer to a thickness sufficient to leave a second layer thickness portion overlying the first layer following a subsequent oxide chemical mechanical polish (CMP) planarization process;

carrying out the oxide CMP process to planarize the second layer and leave the second layer thickness portion; and,

forming metal filled local interconnects extending through a thickness portion of the first and second layers.

2. The method of claim 1, wherein the step of forming metal filled local interconnects comprises:

forming local interconnect trenches;

depositing tungsten or an alloy thereof to fill the local interconnect trenches;

carrying out a tungsten CMP process to expose the second layer; and,

carrying out a batch wafer cleaning process.

3. The method of claim 2, wherein the batch wafer cleaning process comprises an HF containing solution.

4. The method of claim 1, wherein the metal is formed of tungsten or an alloy thereof.

5. The method of claim 1, wherein the step of depositing a first layer comprises an HDP-CVD process comprising phosphine (PH_3) source gas.

6. The method of claim 1, wherein the step of depositing a second layer comprises a CVD process selected from the group consisting of PECVD and HDP-CVD.

7. The method of claim 1, wherein the wherein the step of depositing a second layer comprises an in-situ HDP-CVD process with respect to the step of depositing a first layer.

8. The method of claim 1, wherein the first layer is formed with a phosphorous content of from about 2.5 weight % to about 4.5 weight %.

9. The method of claim 1, wherein the second layer comprises undoped SiO_2 selected from the group consisting of USG, PEOX, and PETEOS oxide.

10. The method of claim 1, wherein the first layer is deposited to a thickness of about 4000 to about 6000 Angstroms.

11. The method of claim 1, wherein the second layer is deposited to a thickness of about 4000 to about 6000 Angstroms.

12. The method of claim 1, wherein the second layer thickness portion is from about 500 Angstroms to about 1000 Angstroms.

13. A method of forming local interconnect (LI) dielectric layer stack to allow improved control over thickness and reduced metallic residue comprising the steps of:

providing a semiconductor substrate comprising CMOS transistors comprising gate electrode portions;

depositing a first layer comprising phosphosilicate glass (PSG) over the semiconductor substrate to a thickness sufficient to fully cover the gate electrode portions including intervening gaps;

depositing a second layer of undoped SiO_2 over and contacting the first layer to a thickness sufficient to leave a second layer thickness portion overlying the first layer following a subsequent oxide chemical mechanical polish (CMP) planarization process;

carrying out the oxide CMP process to planarize the second layer and leave the second layer thickness portion;

forming LI trenches extending through a thickness of the first and second layers;

depositing tungsten to fill the LI trenches; and,

carrying out a tungsten CMP process to expose the second layer.

14. The method of claim 13, further comprising carrying out a batch wafer cleaning process.

15. The method of claim 14, wherein the batch wafer cleaning process comprises etching a portion of the second layer.

16. The method of claim 1, wherein the step of depositing a first layer comprises an HDP-CVD process comprising phosphine (PH_3) source gas.

17. The method of claim 1, wherein the wherein the step of depositing a second layer comprises an in-situ HDP-CVD process with respect to the step of depositing a first layer.

18. The method of claim 1, wherein the step of depositing a second layer comprises a PECVD process.

19. The method of claim 1, wherein the first layer is formed with a phosphorous content of from about 2.5 weight % to about 4.5 weight %.

20. The method of claim 1, wherein the second layer comprises undoped SiO_2 selected from the group consisting of USG, PEOX, and PETEOS oxide.

21. The method of claim 1, wherein the first layer is deposited to a thickness of about 4000 to about 6000 Angstroms.

22. The method of claim 1, wherein the second layer is deposited to a thickness of about 4000 to about 6000 Angstroms.

23. The method of claim 1, wherein the second layer thickness portion is from about 500 Angstroms to about 1000 Angstroms.

24. A local interconnect (LI) dielectric stack comprising:

a planarized first layer of phosphosilicate glass (PSG);

a planarized second layer of undoped SiO_2 overlying and contacting the first layer; and,

tungsten filled local interconnects extending through a thickness of the first and second layers.

25. The local interconnect (LI) dielectric stack of claim 24, wherein the first layer extends above a height of underlying polysilicon electrode gate portions of CMOS transistors.

26. The local interconnect (LI) dielectric stack of claim 24, wherein the second layer is from about 500 Angstroms to about 1000 Angstroms in thickness.

27. The local interconnect (LI) dielectric stack of claim 24, wherein the PSG comprises form about 2.5 weight % to about 4.5 weight % of phosphorous.

28. The local interconnect (LI) dielectric stack of claim 24, wherein the second layer comprises undoped SiO_2 selected from the group consisting of USG, PEOX, and PETEOS oxide.